

HIGH V_{oc} CRYSTALLINE SILICON THIN FILM SOLAR CELLS THROUGH RECRYSTALLISED WAFER EQUIVALENT APPLIED TO SINTERED SILICON

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ABSTRACT: Among Crystalline Silicon Thin-Films (CSiTF), the concept of Recrystallised Wafer Equivalents (RexWE) established by Fraunhofer ISE has steadily shown high efficiencies on good quality substrates. But no low-cost substrate has yet shown high enough results for an industrial launch of this technology. Meanwhile, the recently created company S'TILE has developed a new approach in wafer manufacturing with Sintering of Silicon Powders. It is a cheap process which presents among other advantages the avoiding of sawing kerf loss and the possibility of high throughput of large area wafers. For this reason, sintered silicon wafers have been used as substrates for RexWE.

Up to 9.2 % of efficiency was obtained on non-optimised 4 cm² solar cells with an excellent open circuit voltage of 580 mV. This V_{oc} is the best obtained up to now with this technology with such low-cost substrates. As the RexWE cell process used here has poor optical confinement, the efficiency is likely to dramatically improve with the CSiTF-optimised texturisation and back reflector already developed at Fraunhofer ISE.

These very promising results may thereby open to a new lead in CSiTF and trigger some large scale manufacturing.

Keywords: Crystalline Silicon, Thin Film Solar Cell, Substrates.

1 INTRODUCTION

High-purity silicon material stands for a great part of conventional solar cells production costs, especially with the current silicon feedstock issues. A solution to reduce costs would be to use less of this expensive silicon by making thinner solar cells and use a cheaper substrate as mechanical carrier. Crystalline Silicon Thin-Films Solar Cells (CSiTF) emerge as such an alternative to wafer-based photovoltaic technologies. They make their own of the advantages of silicon technologies including high efficiency, long-term reliability, material abundance and non-toxicity. Moreover they are technologically close to the mainstream of the current industrial cell fabrication processes, consequently they can be more easily adopted by the photovoltaics industry. Because of these similarities, these technologies are often referred to as wafer equivalents.

The data presented here result from a cooperation between the company S'TILE (France), which provides a new type of silicon wafers, and the Fraunhofer ISE (Germany), which brings its complete Recrystallised Wafer Equivalent (RexWE) process.

It has been demonstrated that RexWE leads to high efficiencies solar cells when used on traditional multicrystalline silicon substrates and is transferable into high throughput and low processing costs type of equipments. But it lacks of a suitable cheap substrate. S'TILE has developed such a low cost substrate solution using the sintering of silicon powder. It has also a good potential for industrialisation.

The new device made out of the combination of this substrate and this CSiTF process is being evaluated in this paper. Preliminary results are very promising.

2 THE SINTERED SILICON PROCESS

The compaction and sintering of silicon powders has been first developed and patented in Poitiers University

(France) [1] and the company S'TILE has been created on the basis of the potential of this concept.

Sintered wafers are fabricated by hot-pressing a micrometric silicon powder, the overview of this mechanism is sketched in Fig. 1. The temperature is below the melting point of silicon and the pressure can reach 30-40 MPa. The grain boundary migration resulting from the plastic deformation of grains during sintering causes a densification of the device up to 100% [2]. This process is well-known in the ceramics industry but, to the best of our knowledge, not used at all for photovoltaics except by S'TILE.

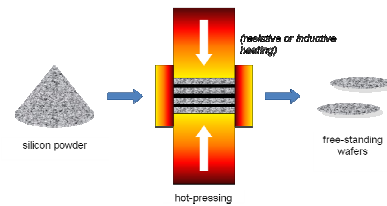


Figure 1: Scheme of the sintering process

The main advantage of this process is that it avoids the silicon waste due to the wire sawing kerf loss, which is typically 150-200 μm thick for each wafer. That is to say, almost as much silicon as in the wafer itself is wasted. This makes the sintering process cost lower than the conventional block casting and sawing process, for a given initial material cost. In addition, any quality of silicon can be used for sintering.

The development of this process, even though it is young, permits currently to monitor the characteristics of the sintered wafer with an excellent repeatability.

The lab-scale presses used currently are able to make up to 15 round wafers of 300 mm of diameter maximum in a batch, which allows the demonstration of the high throughput possibilities of the process. The pilot line which is intended to be constructed would have an even higher throughput. The sizing of the press makes an upper limit to the wafer size but does not determine its

size and shape. This is determined by the piston and matrix shape, and basically any shape can be made.

There is no theoretical limit for the size of the wafer, so that the limitation would be the same as for regular wafers, except for the fact that there is less contingency about silicon consumption. The thickness of the wafer is simply determined by the amount of powder used per wafer. Up to now, wafers as thin as 200 μm have been made.

The doping level can be if necessary increased in-situ to a desired value. It is the case to serve as a substrate for RexWE, the wafers have been doped to a resistivity under 1 $\Omega\cdot\text{cm}$.

Glow Discharge Mass Spectroscopy (GDMS) analyses of the powders and the sintered wafers have shown that this sintering process does not induce contamination, as the impurity contents tend to decrease when the hot-pressing process is applied.

Among the characteristics which can be varied, there is also the density of the sintered wafer. Indeed it is possible to make 100 % dense wafers, just like conventional wafers, as well as 50 % dense wafers, which have the same appearance as denser wafers and seem to be as mechanically resistant as them. The possibility of use of such porous wafers for cell processing is not exploited yet, but it could allow even lower silicon consumption [3].

3 THE RexWE PROCESS

The RexWE is a concept created by Fraunhofer ISE and has been improved for many years now. It has shown an efficiency of 13.5 % on a mc-Si substrate with a clean room cell process [4]. However no wafer equivalent made on low-cost material such as ceramics has been able to conduct to high efficiency cells. This is mostly due to the fact that it is a high temperature approach to CSiTF and there is a mismatch in the thermal behaviour of silicon and ceramics.

Chemical Vapour Deposition (CVD) of silicon is generally the bottleneck of CSiTF throughput. But Fraunhofer ISE has demonstrated the possibility of a high throughput CVD reactor [5]. The other main barrier to industrialisation of such technology is the number of process steps for the realisation of the wafer equivalent. There again, it has been possible to mitigate this issue by the use of a shorten process.

The structure of the version of RexWE used in this test is shown in Fig. 2.

The sintered silicon wafers are covered on one face by an intermediate layer (IL), which in our case is a layer of deposited silicon oxide. Then some p^+ doped silicon is deposited by CVD on the intermediate layer. This layer will be used as a seeding layer for the growth of the active silicon layer, but as-deposited it is not crystalline. This is why a step of Zone Melting Recrystallisation (ZMR) is following. It allows the obtaining of multicrystalline silicon as a seeding for the rest of the wafer. As the SiO_2 layer is electrically insulating, it needs to be open to allow the carrier collection. It is done with Laser Fired rear Access (LFA), which is a punctual laser ablation of the intermediate layer and the seeding layer. Then the absorbing p-type silicon layer is epitaxially grown by CVD on the seeding layer to a thickness of about $\sim 15 \mu\text{m}$.

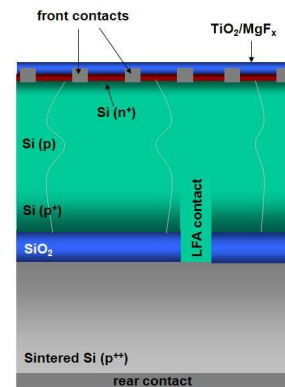


Figure 2: Schematic view of a robust version of a RexWE structure on sintered silicon.

At this stage of the process, the sample is like a regular silicon wafer and can be treated as such by any conventional silicon solar cell process. In this test, the following cell process includes: POCl_3 diffused emitter formation, evaporated and electroplated contacts, remote hydrogen passivation and a double layer antireflection coating. The cells dimensions are 2 x 2 cm^2 ; they are separated from each other which also permits edge isolation.

High temperature cell process steps were not troublesome, given that the RexWE is made out of silicon only.

For this first attempt to make wafer equivalents with sintered silicon wafers a simple and robust variation of the RexWE process has been used. Consequently it was not the best one in terms of efficiency developed by Fraunhofer ISE. In particular, the optical confinement is limited, as there is no front side texturing and the intermediate layer of SiO_2 is a moderate backside reflector.

4 RESULTS

4.1 Recrystallisation results

The ZMR is a process which is very dependant from the substrate. As these substrates are made out of silicon, their behaviour at high temperature is matching the one of the seeding layer, which is not the case for ceramic substrates. Provided that the sintered wafers follow certain specifications, and with a few adjustments in recrystallisation parameters, they behave much alike regular multicrystalline silicon substrates for ZMR.

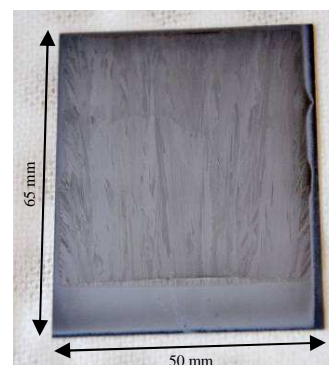


Figure 3: Picture of a recrystallised sample, before LFA and epitaxial growth

For this test, the size of the samples which have been recrystallised is 50 x 65 mm². The grains obtained are up to several mm-wide and several cm-long (Fig. 3).

The whole thickness of the seeding layer is recrystallised. To ensure this, a margin is taken so that the upper part of the substrate is also recrystallised on several tens of microns of depth. The silicon oxide intermediate layer has not moved during the process (Fig. 4).

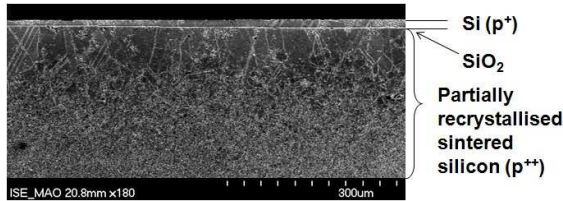


Figure 4: Scanning Electron Microscope view of the cross-section of the wafer after ZMR

4.2 Cell results

The cell results of the best cell obtained are summarized in Table I. As it was a first test, many parameters have been varied from one sample to another, so that there was no batch of many samples. Consequently there is no evaluation of the reproducibility of these results yet, although some other cells presented similar values.

Table I: Best cell characteristics

J_{sc}	V_{oc}	FF	efficiency
21 mA/cm ²	580 mV	75 %	9.2 %

For a preliminary test, the efficiency of 9.2 % is very encouraging. The main element limiting this efficiency is the low short circuit current (J_{sc}). This is mostly due to very little absorption in the long-wavelength range, as the silicon absorbing layer is thin and the reflective properties of the intermediate layer are not optimized.

A high open-circuit voltage (V_{oc}) of 580 mV has been obtained. The fill factor (FF) is good but could be impaired if the current is improved.

5 DISCUSSION

The V_{oc} of 580 mV is a very good value, as CSiTF on low-cost substrates frequently suffer from a too small V_{oc} . This value is the best obtained up to now with this technology applied to such low-cost substrates.

V_{oc} is often a better way to evaluate a CSiTF technology than efficiency, since the latter depends strongly on the details of cell fabrication. On the contrary, V_{oc} describes recombination in the bulk, surface, grain boundary, etc. As such it is more representative of the global material quality [6].

As the RexWE and cell processes used in this test were more focused on simplicity and robustness rather than high efficiency, it is believed that much better results can be obtained.

Especially the optical confinement is poor compared to some variants of the RexWE process. In our case there is no front side texturing and the back side of the active

layer consists in a single layer SiO₂. Fraunhofer ISE has already designed a variant of the RexWE with higher optical confinement [7]. It features plasma texturization, which is very suitable to CSiTF as it etches very little of silicon while lowering the reflection. Also a SiO₂/SiC/SiO₂ stack as intermediate layer, which combines high reflection for long wavelengths and good properties for recrystallisation can be implemented. This design has shown an increase of more than 2 % absolute in cell efficiencies on other substrates [7], and is still being improved.

Another way which can be investigated to improve cell efficiency will be refining of the parameters for ZMR, including the seeding layer thickness. Also, the thickness and the doping level of the epitaxial layer are essential characteristics for internal quantum efficiency of the cell. They may need to be adjusted to the optimum while optical confinement is improved.

In this test, good quality silicon was used for sintering the substrates, and this process was already of a lower cost than with multicrystalline silicon made out of a similar feedstock. Using metallurgical grade silicon could be a way to reduce the cost per watt peak even more, as the intermediate layer of the RexWE would anyway prevent impurities diffusion.

These sintered silicon wafers have also been used for a conventional solar cell process, after ZMR of the whole thickness of the sample. This different route also led to good efficiencies [8].

6 CONCLUSIONS

In this paper, we have seen that a new type of CSiTF cells has been made, combining sintered silicon as a low-cost substrate with recrystallised wafer equivalent process.

Cells made from a non optimised process led to an efficiency of 9.2 % and a V_{oc} of 580 mV. It is a very encouraging result as it indicates that the sintered silicon substrate is appropriate to obtain high quality wafer equivalents. With the already designed high efficiency version of the RexWE process, efficiency is expected to rise of 2-3 % absolute, and more research on this technology could improve it even further. Good efficiencies with this low-cost route could be the trigger to industrialisation of wafer equivalents.

7 ACKNOWLEDGEMENTS

This work was supported by Emertec, OSEO and the Poitou Charente region in France.

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